Marvell 美满电子 2021 校园招聘

Essential technology, done right

Physical Design Engineer

Location: Shanghai

Responsibilities:
Marvell ASIC Chip Design Engineers are working on cutting edge SoC (System on a Chip), ASIC, High Performance Processor, Digital/Analog and Mix-signal Circuit IP design for our clients inside and outside of Marvell. By employing the industry leading tools, methodology, and advanced technologies, the intern will be participating in the delivery of end to end solutions including Chip planning, DFT design, advanced clock tree build, Place&Route implementation and optimization, Methodology development and deployment, as well as Chip hardware validation.

Requirements:
1. Bachelor/Master Degree in Electronics/Electrical Engineering or related fields with coursework in digital logic design, computer architecture, programming/coding, and networking preferred.
2. Research and development experience in one or more of the following areas:
• ASIC Back-end design methodology: Knowledge of synthesis, timing, DFT, floorplanning, physical design, signal/power integrity, packaging, and other back-end activities.
• Architectural design, analysis, and optimization
• SoC design methodology: Knowledge of SoC integration, modeling and verification at different abstract level
• Electronic Design Automation algorithm, tool, and methodology development
• Digital logic implementation and verification on the basis of the target system specification
3. Good software background and strong programming/script languages is a plus.
4. Good English/communication skill and willingness to work with a global team. Skill of other languages will be a good plus.
5. Good learning competency and be able to work in diverse areas in a flexible environment

请将简历命名为"姓名+学校+岗位"投递至邮箱： 448849286@qq.com
或点击链接，投递简历 ：https://jinshuju.net/f/hz7mRU